Electronic Characterization of SiGe Channel Nano-Scale FinFETs

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Abstract. The present work presents a comparative theoretical analysis of SiGe channel nano scale FinFET devices. FinFETs provide a better gate control over channel region than conventional planner MOSFETs and hence are better suited for sub 100 nm device architectures. SiGe material shows higher mobility and lower effective masses of charge carrier and is utilized to provide efficient transport characteristics of electrons in channel area of FETs. The proposed device architecture is incorporated with SiGe channel. A theoretical analysis is performed in order to understand device performance with different Ge mole fractions in SiGe channel region of FinFETs. The SiGe channel FinFET shows better ON state characteristics than conventional Si channel FinFET. Silvaco ATLAS simulator is used with appropriate models to implement and characterize all device structures. This work would be useful in selecting the mole fraction in application specific SiGe channel Transistors.

INTRODUCTION

Device scaling has been a pilot force in VLSI research for the past few decades. Device scaling not only increases chip density but also increases the switching speed of an individual device. On the other hand, by shrinking the size of the device, power consumption of the device also decreases. Many more benefits of device scaling have been proved by researchers. To make the MOSFET a low power high switching speed device, the sub-threshold swing (SS) also needs to be reduced along with the optimization of other physical and electrical parameters. For optimizing the SS, the substrate doping is increased in MOSFET, it also reduces the mobility of the charge carrier, and the ON current of the MOSFET is reduced\textsuperscript{[1]}. A greater amount of substrate doping also increases the leakage current in the MOSFET. For this reason, there is a need to increase the mobility of the charge carrier in the substrate region keeping the value of the SS parameter in limit. For this, many researchers have discovered and presented many techniques. Across all these techniques, channel engineering is a strong contender for increasing charge carrier mobility. MOSFET device has dominated VLSI industry since its origin. The 3-dimensional (3D) version of the MOSFET device, in which the channel or fin region is covered by a gate from 2 or more directions, is called a FinFET. Because of its architecture, FinFET exhibits better electrical performance than 2D MOSFETs\textsuperscript{[2]}. So in this work, the channel engineering with SiGe material is analyzed in FinFET device.

With scaling of the MOSFET, the channel length falls into the short channel region. Here carrier shows quasi-ballistic behavior\textsuperscript{1}. The current in the MOSFET is formulated by following

\[ I_{on} = qN_s V_{inj} \frac{1 - r}{1 + r} \]  

(1)

Here \( V_{inj} \) is the injected velocity of the carrier, at the source end of the channel which can be increased by reducing effective mass of charge carrier. \( r \) is the back scattering rate at source end of channel, that depends on the charge mobility in the channel region.

Although Ge Channel devices display better carrier mobility, while on the other hand the basic properties of Ge material such as low intrinsic band gap and high permittivity, show an increase in short channel effects (SCE), poor Drain Induced Barrier Lowering (DIBL) and high off state leakages in the device\textsuperscript{[4]}. 
In order to achieve higher ON current and to have better switching characteristics of MOSFET SiGe material is utilized. SiGe device provides high carrier mobility and low effective mass of charge carrier. As a result, the ON current of the transistor increases and the SiGe transistor provides better switching characteristics with suppressed SCEs than its conventional versions [5].

**SIMULATION AND RESULTS**

SiGe channel FinFET of 30 nm channel length is analyzed which is shown in the Fig. 1(a). A SiGe layer having cross section of 7x6 nm is sandwiched under a 1 nm SiO2 layer. Two n-doped Si material regions with \( N_d=1\times10^{20} \) cm\(^{-3} \) have been used to implement Source Drain regions. The channel region is left undopped which leads to minimized possible physical device parameter variations in any circuit. The three dimensional architectures of device are created and simulated using Silvaco ATLAS. In order to include physical and electrical effects of nano scale device dimensions, the Schrodinger-Poisson model is used.

![Figure 1(a): SiGe Channel short channel FinFET device architecture (Air hidden); Figure 1(b): \( I_D-V_{GS} \) characteristics of Si\(_{1-x}\)Ge\(_x\) channel FinFET for different values of x.](image)

The 30 nm SiGe channel FinFET is simulated with different mole fractions. For \( I_D-V_{GS} \) curves drain voltage is set to 0.1 V, and gate voltage is varied from 0 to 0.8 V. Figure 1(b) shows a comparative analysis of these simulation results. As the Ge content in the channel region increases, the mobility of charge carriers also increases, resulting in SiGe channels exhibiting comparatively better charge carrier transport properties. This observation reports that, as the Ge content in the FinFET device increases, the drain current also increases. The high mobility provided by the SiGe channel also results in an increase in transconductance of the device (Fig. 2(a)). In order to incorporate, current industry demands transistors with small \( V_{th} \), high \( V_{TH} \) and low SS are required [3]. The Ge content in channel region provides poor subthreshold performance. Further alloy scattering also minimizes the expected theoretical improvements in electrical performance of SiGe channel devices. The threshold voltage \( V_{TH} \) of FinFET device decreases with an increase in Ge fraction of channel region (Fig. 2(a)). This is why, the Ge fraction in the channel region should be chosen carefully, according to the need of application/s.

Multi gate transistors and FinFETs provide steeper SS in comparison to the conventional single gate FETs [6]. However in the nano scale SiGe channel FinFET itself, an exponential growth is noted in the subthreshold slope with increasing Ge fraction in the channel (Fig. 2(b)). DIBL is also a crucial SCE parameter and needs to be handled properly while scaling the device in sub 100 nm dimensions. While on the one hand the Ge variant improves the ON characteristics of the device, making it suitable for high speed applications [7], on the other hand it also gives a rise to the DIBL effect in the device. The Fig. 2(b) shows the DIBL variation in 30 nm FinFET with channel region Ge content.
CONCLUSION

Nano scale FinFET device architectures are investigated using TCAD. The short channel devices are simulated using Schrodinger Poisson model in order to incorporate quantum effects evident in sub 100 nm devices. The comprehensive analysis shows a significant increase in transconductance and $I_{ON}$ of FETs with Ge fraction. Further low band gap of Ge material and alloy scattering in SiGe channel FinFETs result in a poor DIBL and SS. This work hence can be utilized in optimums the Ge mole fraction for $Si_{1-X}Ge_X$ channel nano channel FETs.

REFERENCES